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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/750,200	12/27/2000	Chih-Jen Lin	42390.P9480	7005

7590 08/27/2003

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EXAMINER
DINH, PAUL

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 08/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/750,200	LIN ET AL.	
	Examiner	Art Unit	
	Paul Dinh	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspond nc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

The drawings filed on 12-27-00 are acceptable subject to correction of the informalities indicated on the attached "Notice of Draftsperson's Patent Drawing Review," PTO-948. In order to avoid abandonment of this application, correction is required in reply to the Office action. The correction will not be held in abeyance.

Claim Objections

Claims 2, 13 are objected to because "a switch" should be changed to - - a [switch] multiplexer - - for clarification/accuracy and less confusing; see multiplexer symbol 152 in fig 2.

Claim 13 is objected to because "of the type" should be deleted; it is not clear what is meant by "of the type" or what type the applicant wants to recite.

Claim 16 is objected to because "the control generating circuit" lacks antecedent basic. It seems that the applicant means "the control signal generating unit" as recited in claim 15

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Koenemann Et al (USP 5612963) who discloses a circuit/method comprising:

(Claim 1 and similarly recited claims 10, 15)

an on-die (see on-chip and IC chip in abstract/background/summary/c4-5, 8 for all on-die/on the die/IC die limitations) weight generator circuit to provide at least one weighted test data bit stream for an on die scan chain (fig 2-4) wherein the weight of a test data bit of each of said data bit stream depends upon a corresponding data field downloaded to the weight generator circuit of a data set (fig 2-4);

a memory to store the data set (fig 4);

a data down load circuit to down load each data field of the dataset from the memory to the weight generator circuit in synchronization with the weight generator circuit providing the corresponding test data bit to each said test data bit stream (fig 2-4).

(Claims 2, 13) the weight generator circuit includes a switch (multiplexer/select in fig 2) to generate each weighted test data bit, the switch having an input of a plural number of differently weight bit stream and a control signal of the corresponding data filed (fig 2-4)

(Claims 3-4, 11-12) the memory/data download circuit/weight generating unit/circuit is/are on-die/disposed on IC die (see on-chip in abstract/background/summary/c4-5, 8 and fig 2-4)

(Claim 5) the memory further is to stored at least on other data set; and the data download circuit is to download each data filed of each of the data set in synchronization with the weight generator circuit providing the corresponding test data bit to each said test data bit stream for each data set (fig 2-4)

(Claim 6) the data down load includes:

a control circuit to read each data field of the data set from the memory to a buffer system (fig 2-4) and the buffer system (32) to output each data field from the from the data down load circuit to the weight generator circuit

(Claims 7, 9) the buffer is to output the first the first data to the weight generator circuit in response to a signal from the control circuit (fig 2-4)

(Claims 8, 14) each data field consist of a first range of bit and the data download includes a control circuit to read a data of the data set from the memory at a second ranged of bits at a second time period to a buffer circuit, and the buffer circuit to output each data field from the data down load circuit to the weight generator circuit at a second time periods (fig 2-4)

(Claim 16) the control [generating circuit] signal-generating unit includes both a memory unit and a control circuit (fig 2-4) to download each of the stored control signals from the memory unit (fig 4) to the weight generator circuit in synchronization with the weight generator circuit-determining bit (fig 2-4)

(Claim 17) the memory unit (fig 4) is a memory unit of the IC.

2. Claims 1-5, 10-13, 15-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Motika et al (USP 5983380) who discloses a circuit/method comprising:

(Claim 1 and similarly recited claims 10, 15)

an on-die (see on-chip/IC chip/embedded in c6 and fig 5-6 for all on-die/on the die/IC die limitations) weight generator circuit to provide at least one weighted test data bit stream for an on die scan chain (fig 2-6) wherein the weight of a test data bit of each of said data bit stream

depends upon a corresponding data field downloaded to the weight generator circuit of a data set (fig 2-6);

a memory to store the data set (fig 5-6/claim 9);

a data down load circuit to down load each data field of the dataset from the memory to the weight generator circuit in synchronization with the weight generator circuit providing the corresponding test data bit to each said test data bit stream (fig 2-6).

(Claims 2, 13) the weight generator circuit includes a switch (multiplexer/select in fig 2-6) to generate each weighted test data bit, the switch having an input of a plural number of differently weight bit stream and a control signal of the corresponding data filed (fig 2-6)

(Claims 3-4, 11-12) the memory/data download circuit/weight generating unit/circuit is/are on-die/disposed on IC die (see on-chip/IC chip/embedded in c6 and fig 2-6)

(Claim 5) the memory further is to stored at least on other data set; and the data download circuit is to download each data filed of each of the data set in synchronization with the weight generator circuit providing the corresponding test data bit to each said test data bit stream for each data set (fig 2-6)

(Claim 16) the control [generating circuit] signal generating unit includes both a memory unit and a control circuit (fig 5-6) to down load each of the stored control signal from the memory unit to the weight generator circuit in synchronization with the weight generator circuit determining bit (fig 2-6)

(Claim 17) the memory unit (fig 5-6) is a memory unit of the IC.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Dinh whose telephone number is (703) 305-5662. The examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (703) 308-1323. The fax number for the organization handling this application is (703) 872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Paul Dinh
Patent Examiner
August 14, 2003

MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800